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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,432	09/18/2003	Vishwas V. Hardikar	004.0108	8321
29906 7590 06/26/2007 INGRASSIA FISHER & LORENZ, P.C. 7150 E. CAMELBACK, STE. 325 SCOTTSDALE, AZ 85251			EXAMINER LEADER, WILLIAM T	
			ART UNIT 1753	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.		Applicant(s)	
	10/666,432		HARDIKAR, VISHWAS V.	
	Examiner		Art Unit	
	William T. Leader		1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 October 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>9/18/2003</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Receipt of the papers filed on October 16, 2006, is acknowledged. Applicant has elected without traverse to prosecute Group I, claims 1-19. Nonelected claims 20-70 have been canceled. In addition, applicant has elected species (ii) directed to electrochemical mechanical deposition, and identified claims 1-16 and 18-19 as being readable on the elected species. It has been found that both species may be expeditiously examined at the same time. Claims 1-19 are under consideration.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 5, and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Basol et al (6,942,780) combined with Aaltonen et al (7,220,451) or the Oliver Chyan et al article "Electrodeposition of Copper Thin Film on Ruthenium".

4. The Basol et al patent is directed to a process for electroplating a metal such as copper onto the surface of a semiconductor wafer to form interconnections. The copper is deposited over barrier and seed layers. A typical seed layer material is copper. (column 1, lines 20-48). The seed layer is exposed to a plating solution that contains copper, a suppressor, an accelerator and chloride (electrolyte). See column 2, lines 44-51. This corresponds to the first step of

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instant claim 1. Plating is initialed by applying a potential difference between an anode and electric contact members which carry plating current to the wafer (column 9, lines 13-15). By applying a known potential, a known current is applied since voltage and current are related. This corresponds to the second step of claim 1. Plating is carried out until the desired deposit is formed. See figure 11C. This corresponds to the last step of claim 1. As shown in figure 10B, the process may be carried out with a gap between shaping plate 114 and the front surface of the wafer. The gap may be reduced to zero and the front surface contacted with the upper surface 119 of the shaping plate. In this case the shaping plate may be made of a polishing pad. See column 13, lines 32-38. This embodiment of the process of Basol et al (when the pad contacts the wafer) is an electrochemical mechanical deposition process.

5. The process recited in instant claim 1 differs from that of Basol et al by reciting the electrodeposition of copper on a noble metal layer of a workpiece. As noted above, Basol et al disclose plating on a seed layer which is typically made of copper. The Aaltonen et al patent is directed to a process for depositing a thin metal film. Aaltonen et al observe that in the metallization of integrated circuits, an appropriate seed layer is required. As in Basol et al, Aaltonen et al note that copper is typically used as a seed material. Aaltonen et al disclose that a general problem with copper seeds is their easy oxidation, and teach that noble metals, which do not oxidize easily on their surface, can serve as good seed layers for copper electrodeposition. See column 2, lines 1-14. The seed layer may consist of ruthenium. Column 9, lines 40-50.

6. The Chyan et al article is directed to the electrodeposition of copper on ruthenium and suggests the substitution of a ruthenium for the tantalum nitride/copper barrier/seed layers

typically used in the metallization of integrated circuits. Copper deposition on Ru can be precisely controlled, exhibits a favorable Cu(111) texture, and provides strong copper adherence. See page C347 and the conclusions on page C350.

7. The prior art of record is indicative of the level of skill of one of ordinary skill in the art.

It would have been obvious at the time the invention was made to have utilized a noble metal such as ruthenium as the seed layer, or barrier/seed layer combination, in the process of Basol et al because ruthenium is less easily oxidized than the typical copper seed layer and provides a good base for forming an adherent copper deposit as taught by Aaltonen et al or Chyan et al.

This substitution results in the electrodeposition of copper onto noble metal as recited in instant claim 1. Additionally, it would have been obvious to have utilized the plating process of Basol et al to have provided the copper metallization taught by Aaltonen et al or Chyan et al because a uniform deposit as shown in figure 11C of Basol et al would have been obtained.

8. With respect to claim 7, Basol et al discloses the inclusion of chloride ions in the copper plating bath (column 2, lines 45-50). With respect to claims 17 and 18, as noted above, the process of Basol et al may be carried out without mechanical contact to the surface of the wafer, or with contact by a polishing pad as an electrochemical mechanical deposition process. With respect to claim 19, Basol et al recognize that the thickness of the deposited layer on the tops of the insulating layer should be minimized (column 13, lines 45-48). Choice of a layer thickness within the range recited in claim 19 would have been obvious since Basol et al teach that the layer should be thin.

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9. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Basol et al (6,942,780) combined with Aaltonen et al (7,220,451) or the Oliver Chyan et al article "Electrodeposition of Copper Thin Film on Ruthenium" as applied to claims 1, 5 and 17-19 above, and further in view of Landau (6,261,433).

10. The Landau patent is directed to electrochemical deposition to metallize semiconductor substrates. As shown in figure 1C, copper seed layer 21 is deposited over barrier layer 20. Landau et al teach that other metals, particularly noble metals, can be used for the seed layer (column 3, lines 11-16). Landau et al teach that because the resistive substrate effect is dominant during the beginning of the plating cycle, a relatively low current density, preferably about 5 mA/cm² is applied during the initial plating. The low current density provides very conformal plating substantially uniformly over the plating surface (column 16, lines 33-38). It would have been obvious to have initiated the copper plating in the process of Basol et al at a current density no greater than 20 mA/cm² as taught by Landau et al because the deposit would have been formed uniformly.

11. Claims 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Basol et al (6,942,780) combined with Aaltonen et al (7,220,451) or the Oliver Chyan et al article "Electrodeposition of Copper Thin Film on Ruthenium" as applied to claims 1, 5, and 17-19 above, and further in view of Step et al (6,610,192)

12. As shown in figures 11A-11C of Basol et al, the features of the semiconductor wafer being metallized include a narrow via and a wide trench. An objective of Basol et al is to form a

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uniform deposit while minimizing the deposition on the top surface regions between the features (column 1, line 64 to column 2, line 4). As previously noted, the electroplating bath of Basol et al includes an accelerator and a suppressor. The suppressor molecules attach themselves to the top of the via 14 shown in figure 1C to suppress the material growth thereabouts. These molecules cannot effectively diffuse to the bottom surface of the via through the narrow opening. Preferential adsorption of the accelerator on the bottom surface of the via results in faster growth in that region, resulting in bottom-up growth. See column 2, lines 52-63. Claims 9-16 differ from the process of Basol et al by reciting specific suppressor and accelerator compounds.

13. The Step et al patent is directed to a copper electroplating bath useful for filling the small features of an integrated circuit device with copper metallization (column 2, line 66 to column 3, line 7). The integrated circuit includes features such as trenches and vias. See column 4, lines 18-26. The bath is useful in plating on substrates that have apertures that are $\leq 2 \mu\text{m}$ as well as other features that are $>2 \mu\text{m}$ in size (column 4, line 56 to column 5, line 13). This size range corresponds to the feature size recited in instant claims 10 and 14. The plating bath of Step et al may include a suppressor and an accelerator. (Step et al use the terms "accelerator" and "brightener" interchangeably. See column 4, lines 36-37). Particularly suitable suppressors include ethylene oxide-propylene oxide copolymers as recited in instant claim 12 (column 8, lines 28-30). A suitable accelerator (brightener) is 1-sodium-3-mercaptopropane-1-sulfonate as recited in instant claim 16. The use of the specific suppressors and accelerators disclosed by Step et al as the suppressors and accelerators in the process of Basol et al would have been obvious because these particular compounds are effective in filling trenches and vias. Since the

bath formulation suggested by the references is the same as that recited by applicant, the function of the formulation would have been expected to be the same as that recited.

Double Patenting

14. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

15. Claims 6-8 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-39 of U.S. Patent No. 7,105,082 to Hardikar in view of Aaltonen et al (7,220,451) or the Oliver Chyan et al article "Electrodeposition of Copper Thin Film on Ruthenium". Instant claim 6 recites providing an anion in the electrodeposition composition in an amount sufficient to lower the cloud point of the suppressor to approximately no greater than the electrodeposition temperature. The claims of the Hardikar patent are directed to an electrodeposition composition and electrodeposition method in which an anion is present in

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an amount to lower the cloud point of the suppressor to a temperature approximately no greater than the electrodeposition temperature. Instant claims 6 and 7 differ from the claims of the Hardikar patent by reciting depositing copper on a noble metal layer. Aaltonen et al and the Chyan et al article are taken as above. It would have been obvious to have modified the claimed process of Hardikar by utilizing a noble metal such as ruthenium for the seed layer or combination barrier/seed layer as taught by Aaltonen et al and Chyan et al because ruthenium is less easily oxidized than the typical copper seed layer and provides a good base for forming an adherent copper deposit as taught by Aaltonen et al or Chyan et al.

Claim Rejections - 35 USC § 112

16. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13 contains the trademark/trade name Pluronic®, Pluronic®R, Tetronic® and Tetronic®R. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the

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trademark/trade name is used to identify/describe a composition and, accordingly, the identification/description is indefinite.

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Chen et al patent (6,974,771) is directed to a method for forming a barrier layer in high aspect ratio vias. Chen et al teach that the seed layer in formed in the via may comprise ruthenium or a ruthenium alloy (column 16, lines 18-20). The Becking patent (5,525,207) is directed to glycol compounds and teaches that the cloud point of a compound is the temperature at which the compound begins to precipitate out of solution at a given concentration and solvent mixture (column 1, lines 37-39).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 571-272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



William Leader
June 18, 2007



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